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A Flexible Low-Cost, High-Precision, Single Interface Electrical Impedance Tomography System for Breast Cancer Detection Using FPGA

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Abstract. Typically, in multi-frequency Electrical Impedance Tomography (EIT) systems, a current is applied and the voltages developed across the subject are detected. However, due to the complexity of designing stable current sources, there has been mention in the literature of applying a voltage to the subject whilst measuring the consequent current flow. This paper presents a comparative study between the two techniques in a novel design suitable for the detection of breast cancers. The suggested instrument borrows the best features of both the injection of current and the application of voltage, circumventing their limitations. Furthermore, the system has a common patient-electrode interface for both methodologies, whilst the control of the system and the necessary signal processing is carried out in a field programmable gate array (FPGA). Through this novel system, wide-bandwidth, low-noise, as well as high-speed (frame rate) can be achieved.

1. Introduction

Electrical Impedance Tomography (EIT) is a technique that determines the electrical conductivity distribution within the volume of a subject under test, by collecting measurements of current or measurements taken at its surface, based on induced stimuli. The solution of this inverse problem is further used to reconstruct an image of this distribution [1]. In general, there are two methodologies for the design of the signal source, and the relevant measurement systems, associated with the development of EIT devices [2]. First, using a voltage source can reduce the difficulty and cost of the design, it is relatively easy and quick to calibrate, but suffers from increased sensitivity to high frequency noise [3]. The second possibility is using a current source, which, for stability, requires complex circuitry for trimming to achieve high output impedance, [3], as a precision current source for EIT requires output impedance much higher than that of the load, over a significant frequency bandwidth. This is by far the most common method of choice, due to its high noise immunity [4]. Ideally, one would like the simplicity of voltage sources with the noise advantages of a current source. As discussed, in this paper we will be presenting a system that is under development that uses the approach of both kinds of signal sources, controlled by an FPGA, so that it can meet very stringent specifications.

2. System overview

We are developing an EIT system based on both voltage and current source methods in a single patient interface. Both systems share a common main platform for signal generation and control, based on a field programmable gate array (FPGA) with embedded digital signal processing (DSP). The analogue subsystem comprises (in order) a DAC, the signal generators (voltage and current), a single patient-electrode interface for both types of signal, a PGA and finally an ADC. The system can accurately measure a load impedance of 100Ω to 50 KΩ, with a 1% resolution as the minimum difference that can be differentiated. The frequency range the system is expected to cover is 10Hz to 20MHz. In order to measure impedances in several frequencies, we implemented a multi frequency waveform generator and a phase-sensitive demodulator inside a Xilinx Virtex-5 FPGA for design flexibility and scalability, as well as for control of the multiplexers to select electrodes to achieve a system with low noise and high speed.

3. Analogue sub-system

The developed analogue sub-system in the EIT system shown in Figure 1 consists of a DAC, a current injection and a separate voltage applying sub-system that are linked to separate measurement systems. Suitable converters from measured current to voltage are also part of the system, and the results are taken to programmable gain amplifiers before being passed to the ADC, and finally to the FPGA for demodulation. Work is in progress on the design a multi-frequency constant current and voltage source, V-I converter suitable for the current source and an I-V converter for current measurement. Figure.2 illustrates the system architecture. Please note the separate voltage and current sources [6].

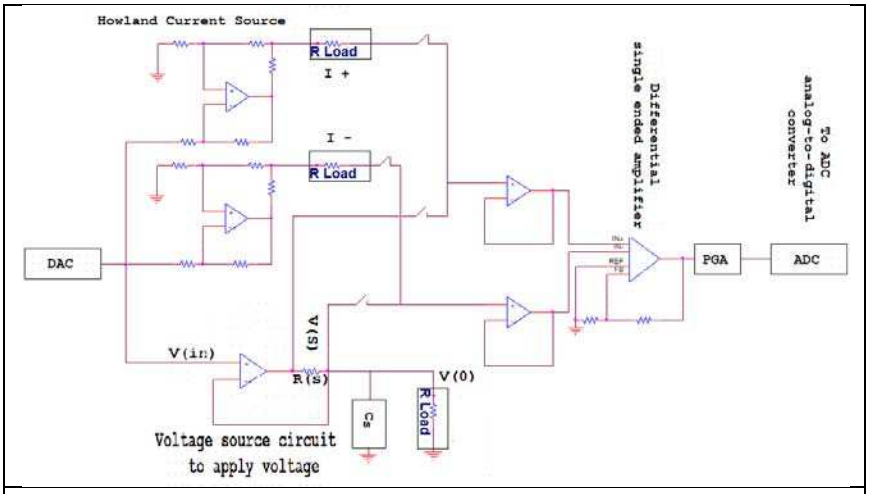


Figure 1 Current and Voltage source circuit with measurement system

The output of the DAC is fed to either the voltage or current sources. When current or voltage is applied to the electrode, voltages (or current I-V converters from R_s) are produced. In the acquisition system, the voltmeters measure single-ended differential voltages, which are developed between electrodes. Then, the voltage difference through a PGA feeds the result to a 16-bit ADC [7] [8]. Then the output is transferred to the FPGA for digital PSD and then by the digital matched filter to extract the real and imaginary components.

4. FPGA control and generator module

4.1. FPGA design

As illustrated in figure 2, in the digital sub-system, the design consists of a signal generator based on a direct digital synthesizer (DDS) module for multi-frequency signal generation by a look-up table (LUT). The DDS is also used to produce the reference signal for the phase-sensitive demodulation (PSD) block. To improve the speed of the system, the digital (PSD) is realized in the FPGA with

digital embedded signal processor components (DSP48). The variable precision that can be achieved by the use of an FPGA ensures that our system can reach the accuracy required by EIT.

4.2. Signal generator

The control module of the direct digital synthesizer (DDS) is used to generate a suitable phase argument that is mapped by the look-up table to the desired output waveform, a sine-wave in this case. After that the DDS presents these samples to a digital-to-analogue converter (DAC), external to the FPGA, and a low-pass filter to obtain an analogue waveform with the specific frequency structure. Output frequency, f_{out}, of the DDS waveform is a function of the system clock frequency f_{clk}, and the number of bits $B_{\Theta(n)}$ in the phase increment value $\Delta\theta$; that is,[5]

$$f_{out} = f(f_{clk}, B_{\Theta(n)}, \Delta\theta) \quad \text{Thus,} \quad f_{out} = f_{clk}\, \Delta\theta / 2^{[B_{\Theta(n)}]} \text{ Hz} \qquad (1)$$

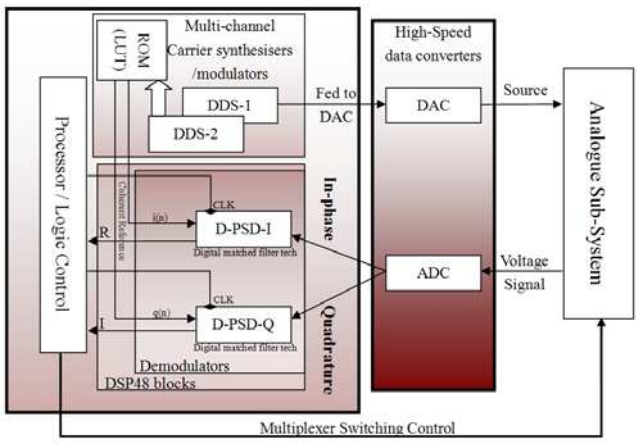
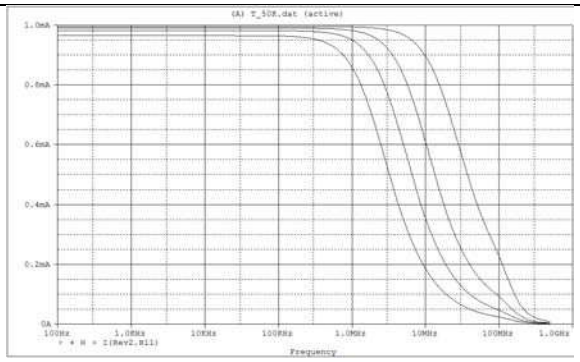


Figure 2 Digital Sub-system and FPGA block diagram



```
Cutoff_Lowpass_3dB(i(Rload))
            R(L) 20k: 20.92856meg
            R(L) 10k: 7.77795meg
            R(L) 5k: 3.85653meg
            R(L) 2k: 1.94947meg
```

Figure 3 Bandwidth of Current source circuit

The off-the-shelf Xilinx Core associated with signal generation runs at a speed of up to 445MHz. As this can be clocked inside the FPGA by a dedicated clock, this speed is more than adequate to provide a signal of 20MHz to meet EIT requirements.

The latency that may be expected by a digital system like the one defined above can affect the acquisition speed of the overall system. The most significant contribution to this latency internally to the FPGA comes from the DDS Core. This latency is the delay from the assertion to the first valid output and the delays from changes to programmable phase increment and offset to a change in output values and especially for multiple channels.

Table 1 frequency latency

$f_{out\ (Hz)}$	**10 KHz**	**100 KHz**	**1 MHz**	**5 MHz**	**10 MHz**	**20 MHz**
Cycles per frequency	10	10	10	10	10	10
Period per cycle	100µsec	10µsec	1µsec	200nsec	100nsec	50nsec
Total latency	1113.5µsec					

For the total latency per frame, the calculation is further complicated by the fact that the circuit sequentially selects electrodes by controlling the channel-selecting multiplexers. Assuming a 4-electrode measurement method is used, and N number of electrode combinations per frame, the

latency is equal to the sum of all the internal delays and external delays per electrode combination, times the number of combinations per frame. As the FPGA is highly parallel, though, it is possible to minimize the external delays caused by the control of the switching mechanism, by pipelining the sending of the command words to the multiplexers with an actual, single electrode combination capture time. As an approximation, the total latency per frame should not exceed 25msec.

4.3. Further FPGA Tasks

The demodulation can again be carried out in the FPGA, and in this case the method to be used is digital quadrature demodulation, returning the In-phase, *i(n)*, and the Quadrature, *q(n)*, components of the complex measurements. Further processing, using the FPGA, returns the amplitude and phase of the measurement.

Within the FPGA the control logic required for the setting of the multiplexers responsible for the channel switching is also implemented.

A single digital sub-system can be developed using a FPGA for both current injection and applying voltage. The advantages of this are a fast system and also the ability to control switching. Ideally, a reconstruction method that can combine both types of measurement should be used, as in trans-admittance systems. However, all the necessary post-processing before reconstruction can and should be run in the FPGA for overall system speed increase. At the same time, the FPGA, ideally suited for a control device, can offer switching of high-channel count systems, in an integrated package.

5. Conclusion

As discussed above, a novel EIT system can be achieved with wide-bandwidth, low-noise, and high-speed by the use of digital techniques. Moreover, this EIT system is not restricting the FPGA only to signal generation and demodulation, but also the full control of the system, especially the electrode switching between channels. In effect, an FPGA can be used to act as the heart of a fast, versatile and scalable EIT system.

6. References

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